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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No. 042390.P5488D6 Total Pages 5

First Named Inventor or Application Identifier Chia-Hong Jan, et al.

Express Mail Label No. EL143553826US

ADDRESS TO:	**Assistant Commissioner for Patents** **Box Patent Application** **Washington, D. C. 20231**

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

1. X Fee Transmittal Form
(Submit an original, and a duplicate for fee processing)

2. X Specification (Total Pages 36)
(preferred arrangement set forth below)
- Descriptive Title of the Invention
- Cross References to Related Applications
- Statement Regarding Fed sponsored R & D
- Reference to Microfiche Appendix
- Background of the Invention
- Brief Summary of the Invention
- Brief Description of the Drawings (if filed)
- Detailed Description
- Claims
- Abstract of the Disclosure

3. X Drawings(s) (35 USC 113) (Total Sheets 10)

4. X Oath or Declaration (Total Pages 7)

a. ___ Newly Executed (Original or Copy)

b. X Copy from a Prior Application (37 CFR 1.63(d))
(for Continuation/Divisional with Box 17 completed) **(Note Box 5 below)**

i. ___ DELETIONS OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).

5. X Incorporation By Reference (useable if Box 4b is checked)
The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

6. ___ Microfiche Computer Program (Appendix)

7. ____ Nucleotide and/or Amino Acid Sequence Submission
(if applicable, all necessary)
a. ____ Computer Readable Copy
b. ____ Paper Copy (identical to computer copy)
c. ____ Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

8. ____ Assignment Papers (cover sheet & documents(s))
9. ____ a. 37 CFR 3.73(b) Statement (where there is an assignee)
____ b. Power of Attorney
10. ____ English Translation Document (if applicable)
11. ____ a. Information Disclosure Statement (IDS)/PTO-1449
____ b. Copies of IDS Citations
12. X Preliminary Amendment
13. X Return Receipt Postcard (MPEP 503) (Should be specifically itemized)
14. ____ a. Small Entity Statement(s)
b. Statement filed in prior application, Status still proper and desired
15. ____ Certified Copy of Priority Document(s) (if foreign priority is claimed)
16. X Other: COPY OF POSTCARD WITH EXPRESS MAIL LABEL

17. **If a CONTINUING APPLICATION,** check appropriate box and supply the requisite information:
___ Continuation X Divisional ___ Continuation-in-part (CIP)
of prior application No: 09/386,495, filed 8/30/99 which is a further divisional of 09/191,729, filed 11/13/98.

18. **Correspondence Address**
____ Customer Number or Bar Code Label ____ (Insert Customer No. or Attach Bar Code Label here)
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Attorney's Docket No.: 042390.P5488D6 Patent

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of:	)	
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JAN, C., et al.	)	
	)	Examiner: Unknown
Serial No: Unknown	)	
	)	Art Unit: Unknown
Filed: Herewith	)	
	)	
For: METHOD AND DEVICE FOR IMPROVED SALICIDE RESISTANCE ON POLYSILICON GATES	)	

BOX: PATENT APPLICATION
Assistant Commissioner for Patents
Washington, D.C. 20231

PRELIMINARY AMENDMENT

Sir:

Prior to an examination of the above-identified application, and prior to calculating the filing fee of the enclosed divisional application, Applicants respectfully request the Examiner to enter the following preliminary amendments and to consider the following remarks.

IN THE CLAIMS:

Please cancel claims 1-7 and 15-122 without prejudice.

IN THE SPECIFICATION

On page 8, at line 32, after "salicide." and before "In", insert the following sentence: "A polycide may also be called a polysilicide. It should be noted that silicides can be self-aligning or non-self-aligning, and if the silicide is self-aligning, it may be called a salicide. It is to be understood by one of ordinary skill in the art that polycides, other than self-aligning silicides, may also be formed."

On page 10, at line 25, after "salicide." and before "In", insert the following sentence: "A polycide may also be called a polysilicide. It should be noted that silicides can be self-aligning or non-self-aligning, and if the silicide is self-aligning, it may be called a salicide. It is to be understood by one of ordinary skill in the art that polycides, other than self-aligning silicides, may also be formed."

On page 12, at line 22, after "salicide." and before "In", insert the following sentence: "A polycide may also be called a polysilicide. It should be noted that silicides can be self-aligning or non-self-aligning, and if the silicide is self-aligning, it may be called a salicide. It is to be understood by one of ordinary skill in the art that polycides, other than self-aligning silicides, may also be formed."

On page 15, at line 11, after "salicide." and before "In", insert the following sentence: "A polycide may also be called a polysilicide. It should be noted that silicides can be self-aligning or non-self-aligning, and if the silicide is self-aligning, it may be called a salicide. It is to be understood by on of ordinary skill in the art that polycides, other than self-aligning silicides, may also be formed."

On page 18, at line 28, after "salicide." and before "In", insert the following sentence: "A polycide may also be called a polysilicide. It should be noted that silicides can be self-aligning or non-self-aligning, and if the silicide is self-aligning, it may be called a salicide. It is to be understood by one of ordinary skill in the art that polycides, other than self-aligning silicides, may also be formed."

REMARKS

This divisional application is being filed in response to an election requirement imposed by Examiner Vu in an Office Action mailed on November 29, 1999, for Application No. 09/386,495, filed August 30, 1999, which is a further divisional of Application No. 09/191,729 filed on November 13, 1998. Applicants have cancelled claims 1-7 and 15-122; claims 8-14 remain pending in this divisional application.

Please enter the amendment before calculating the filing fee of the enclosed divisional application.

Further, Applicants have amended the specification to clarify that a polycide is a shortened general term used to represent the term polysilicide. Further, polysilicide is also a broad term encompassing both non-self-aligned and self-aligned silicides (salicides). Applicants submit that support for the amendments is found in the specification as originally filed, and that no new matter has been added.

Applicants respectfully request consideration of this application in view of the foregoing amendments.

Deposit Account Authorization

Authorization is hereby given to charge our Deposit Account No. 02-2666 for any charges that may be due.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Date: Jan. 4, 2000

Lisa A. Norris
Reg. No. 44,976
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UNITED STATES PATENT APPLICATION

FOR

A METHOD AND DEVICE FOR IMPROVED SALICIDE RESISTANCE ON POLYSILICON GATES

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I hereby certify that I am causing this paper or fee to be deposited with the United States Postal Service "Express Mail Post Office to Addressee" service on the date indicated above and that this paper or fee has been addressed to the Assistant Commissioner for Patents, Washington, D. C. 20231

Dorcas J. Milliken
(Typed or printed name of person mailing paper or fee)

(Signature of person mailing paper or fee)

11/13/98
(Date signed)

A METHOD AND DEVICE FOR IMPROVED SALICIDE RESISTANCE ON POLYSILICON GATES

FIELD OF THE INVENTION

The present invention relates to the field of semiconductor devices. More particularly, the present invention relates to a method and device for improved resistance on gate electrodes. Specifically, the present invention relates to a method and device for improved salicide resistance on polysilicon gates.

BACKGROUND OF THE INVENTION

Transistors are commonly used in semiconductor circuitry to control current flow. For example, a transistor can be used as a switching mechanism to allow the flow of current between a source and a drain region in a circuit when a certain threshold voltage is met. Transistors generally include a gate electrode that allows or prevents the flow of current in the transistor based on applied voltage.

Figure 1a shows a cross-sectional view of a conventional gate electrode 100 formed on a substrate 110, the underlying structure of which is not shown. It should be noted that the figures are merely illustrative and have been simplified for clarity purposes. A thin insulative layer 120 is formed on the substrate 110 to act as a barrier between the substrate 110 and the conductive portions of the gate electrode 100. An example of an insulative layer 120 can be an oxide layer, such as silicon dioxide (SiO_2). Formed on the insulative layer 120 is a gate layer 130. An example of a gate layer 130 can be a polysilicon layer. Formed on the gate layer 130 is a conductive layer 160. An example of a conductive layer 160 can be a polycide layer, such as titanium salicide ($TiSi_2$). When a threshold voltage is applied to the gate layer 130 by the conductive layer 160, current will flow through the gate layer 130. Often insulative spacers 140 and 150 are formed to each side of the gate layer 130 to prevent transfer of current between the gate layer 130 and surrounding structures in the semiconductor.

In semiconductor circuit design, frequently, gate electrodes are designed in long continuous lines on the semiconductor substrate to efficiently provide current to several transistors in a circuit. Currently, improved semiconductor transistor performance is being achieved through device scaling in which the gate layer widths are being reduced from .20 μm to .15 μm and below (sub-.15 μm). As the gate layer width dimensions decrease, so do the conductive layer line widths formed above them.

When the gate layer widths decrease below.20 μm, current process techniques produce conductive lines with sharply increasing resistance. This is detrimental to the efficiency of the semiconductor, as higher resistance decreases the speed of the semiconductor circuitry. Additionally, process yields drop due to defective conductive line formation reducing manufacturing output. These problems have been particularly noted in current fabrication processes where titanium salicide ($TiSi_2$) is formed as the conductive layer in a polysilicon gate.

Figure 1b illustrates a cross-sectional view of a conventional gate electrode 100 formed on a substrate 110, the underlying structure of which is not shown. An example of a gate electrode 100 can be a polysilicon gate electrode. Formed on the substrate 110 is an insulative layer 120. An example of an insulative layer 120 can be an oxide. Formed on the insulative layer 120 is a conductive gate layer 130. An example of a gate layer 130 is a polysilicon layer. Formed on the gate layer 130 is a conductive layer 160. An example of a conductive layer 160 can be a polycide, such as titanium salicide. Insulative spacers 140 and 150 are formed adjacent to the gate layer 130 and conductive layer 160 to prevent current flow between the gate layer 100 and surrounding structures.

During formation of the conductive layer 160, components from underlying gate layer 130 often out diffuse into a reactant layer that is used to form the conductive layer 160. For example, silicon components of an underlying gate layer 130 may out diffuse into the conductive layer 160. This out diffusion results in a conductive layer 160 wider than the gate layer 130. When

the gate layer 100 width is decreased below .20μm, the conductive layer 160 becomes stressed by its enclosure between the side walls of the spacers 140. This results in increased resistance in the conductive layer 160. Increased resistance in the conductive layer directly impacts the quality of the semiconductor circuit. The circuit becomes inefficient and circuit failure or device failure may occur.

Another result of decreasing the gate line widths below .20μm is a decrease in process yields. This is due to non-formation of the conductive layer. This is attributed to the reduced reaction area, or nucleation sites, available at such small dimensions. The reduced dimensions of the gate layer reduces nucleation sites on which the conductive layer can form during processing. Using current process techniques, if sufficient nucleation sites are not provided, the conductive layer often won't form. This directly impacts the semiconductor manufacturer by reducing output.

Based on the above described problems, it would be desirable to have a method and/or device which will improve the polycide resistance in polysilicon gate widths below .20 μm.

BRIEF SUMMARY OF THE INVENTION

The present invention provides a method and a device which improves polycide resistance in gate electrode widths below .20 μm. The invention provides several embodiments one embodiment of which is described below.

In one embodiment of the present invention there is provided a gate electrode comprising a thin insulative layer. A gate layer is formed on the thin insulative layer. A conductive layer is formed on the gate layer. Thick first spacers are formed adjacent to opposite sides of the gate layer. Thick second spacers are formed adjacent to the thick first spacers. The thick first spacers are recessed to create an open space between the gate layer and thick second spacers.

BRIEF DISCUSSION OF THE SEVERAL VIEWS OF THE DRAWINGS

For fuller understanding of the present invention, reference is made to the accompanying drawings in the following detailed description of the invention. In the drawings:

Figure 1(a) is a cross-sectional illustration of a conventional gate electrode in the prior art depicting a non-stressed conductive layer.

Figure 1(b) is a cross-sectional illustration of a conventional gate electrode in the prior art depicting a stressed conductive layer.

Figures 2 (a) - (h) are cross-sectional illustrations of the formation of a gate electrode with a conductive layer and recessed thick inner spacers and non-recessed thick outer spacers.

Figures 3 (a) - (i) are cross-sectional illustrations of the formation of a gate electrode with a conductive layer and recessed thin inner spacers and recessed thick outer spacers.

Figures 4 (a) - (i) are cross-sectional illustrations of the formation of a gate electrode with a conductive layer and non-recessed thin inner spacers and partially recessed outer spacers.

Figures 5 (a) - (m) are cross-sectional illustrations of the formation of a gate electrode with a conductive layer and two spacer stacks. The outermost spacer stack having recessed thin inner spacers and recessed thick outer spacers. The inner spacer stack having non-recessed thin inner spacers and non-recessed thin outer spacers.

Figures 6 (a) - (p) are cross-sectional illustrations of the formation of a gate electrode with a conductive layer and two spacer stacks. The outermost spacer stack having recessed thin inner spacers and recessed thick outer spacers. The

inner spacer stack having recessed thin inner spacers and recessed thin outer spacers.

DETAILED DESCRIPTION OF THE INVENTION

The present invention provides a method and a device to improve polycide resistance on gate electrodes less than .20 μm in width. In the following description of the several embodiments of the invention, numerous details are set forth in order to provide a thorough understanding of the present invention. It will be appreciated by one having ordinary skill in the art that the present invention may be practiced without such specific details. In other instances, well known structures and techniques have not been described in detail in order to avoid obscuring the subject matter of the present invention. It will be understood by those having ordinary skill in the art that the structures of the present invention may be formed by various techniques.

Referring now to the drawings, one embodiment of the present invention is shown in Figures 2a - h. Figure 2a illustrates a gate layer 220 formed on a thin insulative layer 210 on a substrate 200. In one embodiment, the gate layer 220 can be a polysilicon. In one embodiment, the gate layer 220 is less than .20 μm in width. These structures are formed using conventional deposition and etching techniques well-known in the art.

In Figure 2b, a thick first spacer layer 230 is deposited or grown on the gate layer 220 and substrate 200. In one embodiment, the thick first spacer layer 230 can be an oxide. In one embodiment, the thick first spacer layer 230 can be deposited or grown to a thickness in the range of approximately 200 - 600Å, for example, 300Å. It should be noted that the thick first spacer layer 230 can be deposited or grown using deposition techniques that are well known in the art and are not described in detail herein.

In Figure 2c, a thick second spacer layer 240 is deposited or grown on the thick first spacer layer 230. In one embodiment, the thick second spacer layer 240 can be a nitride. In one embodiment, the thick second spacer layer 240 can be deposited or grown to a thickness in the range of approximately 300 - 2000Å, for

example, 800Å. It should be noted that the thick second spacer layer 240 can be deposited or grown using deposition techniques that are well known in the art and are not described in detail herein.

The thick second spacer layer 240 is etched to form the spacer structure illustrated in Figure 2d. In one embodiment, this etch is an anisotropic (directional) etch which will remove nitride, but not oxide. Examples of anisotropic etches are a dry etch or a plasma etch.

The thick first spacer layer 230 is recessed by etching to form the spacer structure illustrated in Figure 2e. The recessing creates an open space between the thick second spacer layer 240 and the gate layer 220. In one embodiment, the thick first spacer layer 230 is etched approximately 60 nm deeper than the surface of the gate layer 220. In one embodiment, the etching forms a space approximately 200 - 600Å, for example, 300Å, between the thick second spacer layer 240 and the gate layer 220. In one embodiment this etch is an isotropic (multidirectional) etch which will remove oxide, but not nitride. Examples of isotropic etches are dry or wet etches. It should be noted that the side walls of the gate layer 220 are now exposed creating a larger contact (reaction) surface area.

In Figure 2f, a reactant layer 250 is deposited, for example by sputter, electron beam evaporation, chemical vapor, or plasma deposition. In one embodiment, the reactant layer 250 can be a metal, such as titanium.

The reactant layer 250 and the gate layer 220 are then annealed to form a conductive layer 260 as shown in Figure 2g. In one embodiment, the formed conductive layer 260 can be a polycide, such as titanium salicide. In one embodiment, the anneal may be performed using a rapid thermal annealing process in a nitrogen ambient. In one embodiment, additional anneals can be performed to decrease the resistance of the conductive layer 260. It is to be noted that the conductive layer 260 can now extend beyond the edges of the gate layer 220 and is not constrained and stressed by the thick first spacer layer 230.

The unreacted portion of reactant layer 250 is etched away leaving the conductive layer 260 as illustrated in Figure 2h. In one embodiment, this etch is an isotropic etch which will remove unreacted titanium, but not titanium salicide.

Another embodiment of the present invention is illustrated in Figures 3 a - i. Figure 3a illustrates a gate layer 320 formed on a thin insulative layer 310 on a substrate 300. In one embodiment, the gate layer 320 can be a polysilicon. In one embodiment, the gate layer 320 is less than .20 μm in width. These structures are formed using conventional deposition and etching techniques well-known in the art.

In Figure 3b, a thin first spacer layer 330 is deposited or grown on the gate layer 320 and substrate 300. In one embodiment, the thin first spacer layer 330 can be an oxide. In one embodiment, the thin first spacer layer 330 is deposited or grown to a thickness in the range of approximately 50 - 300 Å, for example, 100Å. It should be noted that the thin first spacer layer 330 can be deposited or grown using deposition techniques that are well known in the art and are not described in detail herein.

In Figure 3c, a thick second spacer layer 340 is deposited or grown on the thin first spacer layer 330. In one embodiment, the thick second spacer layer 340 can be a nitride. In one embodiment, the thick second spacer layer 340 is deposited or grown to a thickness in the range of approximately 300 - 2000Å, for example, 800Å. It should be noted that the thick second spacer layer 340 can be deposited or grown using deposition techniques that are well known in the art and are not described in detail herein.

The thick second spacer layer 340 is etched a first time to form the structure illustrated in Figure 3d. In one embodiment, this etch is an anisotropic (directional) etch which will remove nitride, but not oxide. Examples of anisotropic etches are a dry etch or a plasma etch.

The thick second spacer layer 340 is then recessed by etching a second time to form the spacer structure illustrated in Figure 3e. In one embodiment, the thick second spacer layer 340 is etched approximately 60 nm deeper than the surface level of the gate layer 320. In one embodiment, this etch is an isotropic (multidirectional) etch which will remove nitride, but not oxide. Examples of isotropic etches are a wet or dry etch.

The thin first spacer layer 330 is then recessed by etching to form the spacer structure illustrated in Figure 3f. In one embodiment, this etch is an isotropic (multidirectional) etch which will remove oxide, but not nitride. Examples of isotropic etches are a dry, wet or chemical bath etch. It should further be noted that the side walls of the gate layer 320 are now exposed creating a larger contact (reaction) surface area

In Figure 3g, a reactant layer 350 is deposited, for example, by sputter, electron beam evaporation, chemical vapor, or plasma deposition. In one embodiment, the reactant layer 350 can be a metal, such as titanium.

The reactant layer 350 and the gate layer 320 are then annealed to form a conductive layer 360 as shown in Figure 3h. In one embodiment, the formed conductive layer 360 can be a polycide, such as titanium salicide. In one embodiment, the anneal may be performed using a rapid thermal annealing process in a nitrogen ambient. In one embodiment, additional anneals can be performed to decrease the resistance of the conductive layer 360. It is to be noted that the conductive layer 360 can now extend beyond the edges of the gate layer 320 and is not constrained and stressed.

The unreacted portion of reactant layer 350 is etched away leaving the conductive layer 360 as illustrated in Figure 3i. In one embodiment, this etch is an isotropic etch which will remove unreacted titanium, but not titanium salicide.

Another embodiment of the present invention is illustrated in Figures 4 a - i. Figure 4a illustrates a gate layer 420 formed on a thin insulative layer 410 on a silicon substrate 400. In one embodiment, the gate layer 420 can be polysilicon. In one embodiment, the gate layer 420 is less than .20 μm in width. These structures are formed using conventional deposition and etching techniques well-known in the art.

In Figure 4b, a thin first spacer layer 430 is deposited or grown on the gate layer 420 and substrate 400. In one embodiment, the thin first spacer layer 430 can be an oxide. In one embodiment, the thin first spacer layer 430 is deposited or grown to a thickness in the range of approximately 50 - 300Å, for example, 100Å. It should be noted that the thin first spacer layer 430 can be deposited or grown using deposition techniques that are well known in the art and are not described in detail herein.

In Figure 4c, a thick second spacer layer 440 is deposited or grown on the thin first spacer layer 430. In one embodiment, the thick second spacer layer 440 can be a nitride. In one embodiment, the thick second spacer layer 440 can be deposited or grown to a thickness in the range of approximately 300 - 2000Å, for example, 800Å. It should be noted that the thick second spacer layer 440 can be deposited or grown using deposition techniques that are well known in the art and are not described in detail herein.

The thick second spacer layer 440 is etched a first time to form the structure illustrated in Figure 4d. In one embodiment, this etch is an anisotropic (directional) etch which will remove nitride, but not oxide. Examples of anisotropic etches are a dry etch or a plasma etch.

The thick second spacer layer 440 is then partially recessed by etching a second time to form the spacer structure illustrated in Figure 4e. In one embodiment, the partial recess creates a thin second spacer wall 470 adjacent to the thin first spacer layer 430. In one embodiment, the thin second spacer wall 470 can be in the range of approximately 50 - 200Å, for example, 100Å, in width

and can extend approximately 60 nm deeper than the surface level of the gate layer 420. In one embodiment, this etch is an anisotropic (directional) etch which will remove nitride, but not oxide. Examples of anisotropic etches are a dry etch or a plasma etch.

Following the partial recessing of the thick second spacer layer 440, the thin first spacer layer 430 is etched to form the spacer structure illustrated in Figure 4f. In one embodiment, this etch is an isotropic (multidirectional) etch which will remove oxide, but not nitride. Examples of isotropic etches are a dry, wet or chemical bath etch.

In Figure 4g, a reactant layer 450 is deposited, for example, by sputter, electron beam evaporation, chemical vapor, or plasma deposition. In one embodiment, the reactant layer 450 can be a metal, such as titanium.

The reactant layer 450 and the gate layer 420 are then annealed to form a conductive layer 460 as shown in Figure 4h. In one embodiment, the conductive layer 460 can be a polycide, such as titanium salicide. In one embodiment, the anneal may be performed using a rapid thermal annealing process in a nitrogen ambient. In one embodiment, additional anneals can be performed to decrease the resistance of the conductive layer 460. It is to be noted that the conductive layer 460 can now extend beyond the edges of the gate layer 420 due to flexibility in the thin spacer walls formed from the thin first spacer layer 430 and the thin second spacer walls 470.

The unreacted portion of reactant layer 450 is etched away leaving the conductive layer 460 as illustrated in Figure 4i. In one embodiment, this etch is an isotropic etch which will remove unreacted titanium, but not titanium salicide.

Another embodiment of the present invention is illustrated in Figures 5 a - m. Figure 5a illustrates a gate layer 520 formed on a thin insulative layer 510 on a substrate 500. In one embodiment, the gate layer 520 can be polysilicon. In one

embodiment, the polysilicon gate layer 520 is less than .20 μm in width. These structures are formed using conventional deposition and etching techniques well-known in the art.

In Figure 5b, a thin first spacer layer 530 is deposited or grown on the gate layer 520 and substrate 500. In one embodiment, the thin first spacer layer 530 can be an oxide. In one embodiment, the thin first spacer layer 530 is deposited or grown to a thickness in the range of approximately 50 - 150Å, for example, 50 Å. It should be noted that the thin first spacer layer 530 can be deposited or grown using deposition techniques that are well known in the art and are not described in detail herein.

In Figure 5c, a thin second spacer layer 540 is deposited or grown on the thin first spacer layer 530. In one embodiment, the thin second spacer layer 540 can be a nitride. In one embodiment, the thin second spacer layer 540 can be deposited or grown to a thickness in the range of approximately 50 - 150Å, for example, 50Å. It should be noted that the thin second spacer layer 540 can be deposited or grown using deposition techniques that are well known in the art and are not described in detail herein.

The thin second spacer layer 540 is etched a first time to form the structure illustrated in Figure 5d. In one embodiment, this etch is an anisotropic (directional) etch which will remove nitride, but not oxide. Examples of anisotropic etches are a dry etch or a plasma etch.

Following the etch of the thin second spacer layer 540, the thin first spacer layer 530 is etched to form the structure illustrated in Figure 5e. In one embodiment, this etch is an isotropic (multidirectional) which will remove oxide, but not nitride. Examples of isotropic etches are dry or wet etches. It should be further noted that at this point in a process flow, implants of dopants can be added to the structure to enhance circuit performance.

In Figure 5f, a thin third spacer layer 550 is deposited or grown. In one embodiment, the thin third spacer layer 550 can be an oxide. In one embodiment, the thin third spacer layer 550 is deposited or grown to a thickness in the range of approximately 50 -300Å, for example, 100Å. It should be noted that the thin third spacer layer 550 can be deposited or grown using deposition techniques that are well known in the art and are not described in detail herein.

In Figure 5g, a thick fourth spacer layer 560 is deposited or grown on the thin third spacer layer 550. In one embodiment, the thick fourth spacer layer 560 can be a nitride. In one embodiment, the thick fourth spacer layer 560 is deposited or grown to a thickness in the range of approximately 300 - 2000Å, for example, 800Å. It should be noted that the thick fourth spacer layer 560 can be deposited or grown using deposition techniques that are well known in the art and are not described in detail herein.

The thick fourth spacer layer 560 is etched a first time to form the structure illustrated in Figure 5h. In one embodiment, this etch is an anisotropic (directional) etch which will remove nitride, but not oxide. Examples of anisotropic etches are a dry etch or a plasma etch.

The thick fourth spacer layer 560 is then recessed by etching a second time to form the spacer structure illustrated in Figure 5i. In one embodiment, the thick fourth spacer layer 560 is etched approximately 60 nm deeper than the surface level of the gate layer 520. In one embodiment, this etch is an isotropic (multidirectional) etch which will remove nitride, but not oxide. Examples of isotropic etches are wet or dry etches.

The thin third spacer layer 550 is then recessed by etching to form the spacer structure illustrated in Figure 5j. In one embodiment, this etch is an isotropic (multidirectional) etch which will remove oxide, but not nitride. Examples of isotropic etches are a dry, wet or chemical bath etch.

In Figure 5k, a reactant layer 570 is deposited, for example, by sputter, electron beam evaporation, chemical vapor, or plasma deposition. In one embodiment, the reactant layer 570 can be a metal such as titanium.

The reactant layer 570 and the gate layer 520 are then annealed to form a conductive layer 580 as shown in Figure 5l. In one embodiment, the conductive layer 580 can be a polycide, such as titanium salicide. In one embodiment, the anneal may be performed using a rapid thermal annealing process in a nitrogen ambient. In one embodiment, additional anneals can be performed to decrease the resistance of the conductive layer 580. It is to be noted that the conductive layer 580 can now extend beyond the edges of the gate layer 520 due to flexibility in the thin spacer walls formed from the thin first spacer layer 530 and the thin second spacer layer 540.

The unreacted reactant layer 570 is etched away leaving the conductive layer 580 as illustrated in Figure 5m. In one embodiment, this etch is an isotropic etch which will remove unreacted titanium, but not titanium salicide.

Another embodiment of the present invention is illustrated in Figures 6 a - p. Figure 6a illustrates a gate layer 620 formed on a thin insulative layer 610 on a substrate 600. In one embodiment, the gate layer 620 can be polysilicon. In one embodiment, the gate layer 620 is less than .20 μm in width. These structures are formed using conventional deposition and etching techniques well-known in the art.

In Figure 6b, a thin first spacer layer 630 is deposited or grown on the gate layer 620 and substrate 600. In one embodiment, the thin first spacer layer 630 can be an oxide. In one embodiment, the thin first spacer layer 630 is deposited or grown to a thickness in the range of approximately 50 - 150Å, for example, 50Å. It should be noted that the thin first spacer layer 630 can be deposited or grown using deposition techniques that are well known in the art and are not described in detail herein.

In Figure 6c, a thin second spacer layer 640 is deposited or grown on the thin first spacer layer 630. In one embodiment, the thin second spacer layer 640 can be a nitride. In one embodiment, the thin second spacer layer 640 can be deposited or grown to a thickness in the range of approximately 50 - 150Å, for example, 50Å. It should be noted that the thin second spacer layer 640 can be deposited or grown using deposition techniques that are well known in the art and are not described in detail herein.

The thin second spacer layer 640 is etched a first time to form the structure illustrated in Figure 6d. In one embodiment, this etch is an anisotropic (directional) etch which will remove nitride, but not oxide. Examples of anisotropic etches are a dry etch or a plasma etch.

Following the etch of the thin second spacer layer 640, the thin first spacer layer 630 is etched to form the structure illustrated in Figure 6e. In one embodiment, this etch is an isotropic (multidirectional) which will attack oxide, but not nitride. Examples of isotropic etches are a dry, wet or chemical bath etch. It should be further noted that at this point in a process flow, implants of dopants can be added to the structure to enhance circuit performance.

In Figure 6f, a thin third spacer layer 650 is deposited or grown. In one embodiment, the thin third spacer layer 650 can be an oxide. In one embodiment, the thin third spacer layer 650 is deposited or grown to a thickness in the range of approximately 50 - 300Å, for example 100Å. It should be noted that the thin third spacer layer 650 can be deposited or grown using deposition techniques that are well known in the art and are not described in detail herein.

In Figure 6g, a thick fourth spacer layer 660 is deposited or grown on the thin third spacer layer 650. In one embodiment, the thick fourth spacer layer 660 can be a nitride. In one embodiment, the thick fourth spacer layer 660 is deposited or grown to a thickness in the range of approximately 300 -2000Å, for example, 800Å. It should be noted that the thick fourth spacer layer 660 can be

deposited or grown using deposition techniques that are well known in the art and are not described in detail herein.

The thick fourth spacer layer 660 is etched a first time to form the structure illustrated in Figure 6h. In one embodiment, this etch is an anisotropic (directional) etch which will remove nitride, but not oxide. Examples of anisotropic etches are a dry etch or a plasma etch.

The thick fourth spacer layer 660 is then recessed by etching a second time to form the spacer structure illustrated in Figure 6i. In one embodiment, the thick fourth spacer layer 660 is etched approximately 60 nm deeper than the surface level of the gate layer 620. In one embodiment, this etch is an isotropic (multidirectional) etch which will remove nitride, but not oxide. Examples of isotropic etches are a wet or dry etch.

The thin third spacer layer 650 is then recessed by etching to form the spacer structure illustrated in Figure 6j. In one embodiment, this etch is an isotropic (multidirectional) etch which will remove oxide, but not nitride. Examples of isotropic etches are dry or wet etches.

At this point, further etches are still to be performed, however, the substrate 600 is left exposed. Thus, if a following etch chemistry is utilized which can remove the substrate 600, the substrate 600 will need to be protected. Thus, a protective layer, for example, an oxide layer, can be provided. The provision of a protective layer is described together with the figures that follow. Alternatively, if a following etch chemistry does not remove the substrate 600, then the process can continue without the necessity of providing and removing a protective layer.

In Figure 6k, a thin protective layer 670 is deposited or grown on the substrate 600. In one embodiment, the thin protective layer 670 can be oxide. In one embodiment, the thin protective layer 670 is deposited or grown to a thickness in the range of approximately 50 -300Å, for example, 50Å. In one

embodiment, the thin protective layer 670 can be an oxide grown by annealing a silicon substrate 600 in an oxygen ambient.

The thin second spacer layer 640 is recessed by etching to form the spacer structure illustrated in Figure 6l. In one embodiment, this etch is an anisotropic (directional) etch which will remove nitride, but not oxide. Examples of anisotropic etches are a dry etch or a plasma etch.

The thin protective layer 670 is removed and the thin first spacer layer 630 recessed by etching a second time to form the spacer structure illustrated in Figure 6m. In one embodiment, the thin first spacer layer 630 is recessed approximately 60 nm deeper than the surface level of the gate layer 620. In one embodiment, this etch is an isotropic (multidirectional) etch which will remove oxide, but not nitride. Examples of isotropic etches are a wet, dry or chemical bath etch. It should be noted that the side walls of the gate layer 620 are now exposed creating a larger contact (reaction) surface area.

In Figure 6n, a reactant layer 680 is deposited, for example, by sputter, electron beam evaporation, chemical vapor, or plasma deposition. In one embodiment, the reactant layer 680 can be a metal, such as titanium.

The reactant layer 680 and the gate layer 620 are then annealed to form a conductive layer 690 as shown in Figure 6o. In one embodiment, the conductive layer 690 can be a polycide, such as titanium salicide. In one embodiment, the anneal may be performed using a rapid thermal annealing process in a nitrogen ambient. In one embodiment, additional anneals can be performed to decrease the resistance of the conductive layer 690. It is to be noted that the conductive layer 690 can now extend beyond the edges of the gate layer 620 and is not constrained and stressed.

The unreacted reactant layer 680 is etched away leaving the conductive layer 690 as illustrated in Figure 6p. In one embodiment, this etch is an isotropic etch which will remove unreacted titanium, but not titanium salicide.

Through out the specification, reference has been made to isotropic and anisotropic etching. It should be noted that the present invention may be performed using these etch processes interchangeably, however, such interchanging of etch processes may cause other complications. The process steps as defined above are the preferred manner in which to perform the present invention.

Additionally, throughout the specification, it has been stated that the etch processes remove only the nitride or oxide layers, however, it should be noted that such etch processes selectively remove the nitride or oxide. In other words, an etch to remove nitride will remove nitride at a faster rate than oxide, such that more nitride is removed and very little oxide is removed; and, an etch to remove oxide will remove oxide at a faster rate than nitride, such that more oxide is removed and very little nitride is removed.

The above described embodiments of the method and device of the present invention provide improved polycide resistance in polysilicon gate widths below .20μm. As earlier described, conductive layers, such as the polycide, titanium salicide, can expand during formation. Previous gate electrode structures had spacer structures which constrained this expansion. This led to a stressed conductive layer that exhibited increased resistance. The several embodiments of the present invention, reduce the stress on the formed conductive layer thereby improving the resistance. In some embodiments, spacers are recessed to remove constraints on the expansion of the conductive layer. In other embodiments, spacers are partially recessed to provide thin spacer walls which flex to dissipate stress. In other embodiments, dual spacer stacks that are recessed and partially recessed also provide dissipate or remove stress on the conductive layer. It is this reduction in the stress by the several embodiments of the present invention, that provides improved resistance. Also, in several of the embodiments the side walls of the gate layer are exposed to allow greater surface area. This aids in formation of the conductive layer by providing for increased nucleation sites. By aiding in formation of the conductive layer, process yields increase.

In the foregoing specification, the invention has been described with reference to specific exemplary embodiments thereof. It will, however, be evident that various modifications and changes may be made thereto without departing from the broader spirit and scope of the invention as set forth in the appended claims. The specification and drawings are, accordingly, to be regarded in an illustrative rather than a restrictive sense.

CLAIMS

What is claimed is:

1. A gate electrode formed on a substrate comprising:
an insulative layer formed on a substrate;
a gate layer formed on the insulative layer;
a conductive layer formed on the gate layer;
thick first spacers formed adjacent to opposite sides of the gate layer wherein the thick first spacers are recessed to create a open space between the both the gate layer and the conductive layer and thick second spacers; and,
thick second spacers formed adjacent to each of the thick first spacers.

2. The gate electrode of claim 1 wherein the insulative layer is an oxide.

3. The gate electrode of claim 2 wherein the gate layer is a polysilicon.

4. The gate electrode of claim 3 wherein the conductive layer is a polycide.

5. The gate electrode of claim 4 wherein the thick first spacers are an oxide.

6. The gate electrode of claim 5 wherein the thick second spacers are a nitride.

7. The gate electrode of claim 6 wherein the polycide is titanium salicide ($TiSi_2$).

8. A gate electrode formed on a substrate comprising:
an insulative layer formed on a substrate;
a gate layer formed on the insulative layer;
a conductive layer formed on the gate layer;
thin first spacers formed adjacent to opposite sides of the gate layer wherein the thin first spacers are recessed; and,

thick second spacers formed adjacent to each of the thin first spacers wherein the thick second spacers are recessed.

9. The gate electrode of claim 8 wherein the insulative layer is an oxide.

10. The gate electrode of claim 9 wherein the gate layer is a polysilicon.

11. The gate electrode of claim 10 wherein the conductive layer is a polycide.

12. The gate electrode of claim 11 wherein the thin first spacers are an oxide.

13. The gate electrode of claim 12 wherein the thick second spacers are a nitride.

14. The gate electrode of claim 13 wherein the polycide is titanium salicide ($TiSi_2$).

15. A gate electrode formed on a substrate comprising:
an insulative layer formed on a substrate;
a gate layer formed on the insulative layer;
a conductive layer formed on the gate layer;
thin first spacers formed adjacent to opposite sides of the gate layer; and,
thick second spacers formed adjacent to each of the thin first spacers wherein the thick second spacers are partially recessed to form thin second spacer walls adjacent to the thin first spacers in a region adjacent to the conductive layer.

16. The gate electrode of claim 15 wherein the insulative layer is an oxide.

17. The gate electrode of claim 16 wherein the gate layer is a polysilicon.

18. The gate electrode of claim 17 wherein the conductive layer is a polycide.

19. The gate electrode of claim 18 wherein the thin first spacers are an oxide.

20. The gate electrode of claim 19 wherein the thick second spacers are a nitride.

21. The gate electrode of claim 20 wherein the polycide is titanium salicide ($TiSi_2$).

22. A gate electrode formed on a substrate comprising:

an insulative layer formed on a substrate;

a gate layer formed on the insulative layer;

a conductive layer formed on the gate layer;

thin first spacers formed adjacent to opposite sides of the gate layer;

thin second spacers formed adjacent to each of the thin first spacers;

thin third spacers formed adjacent to each of the thin second spacers wherein the thin third spacers are recessed; and,

thick fourth spacers formed adjacent to each of the thin third spacers wherein the thick fourth spacers are recessed.

23. The gate electrode of claim 22 wherein the insulative layer is an oxide.

24. The gate electrode of claim 23 wherein the gate layer is a polysilicon.

25. The gate electrode of claim 24 wherein the conductive layer is a polycide.

26. The gate electrode of claim 25 wherein the thin first spacers are an oxide.

27. The gate electrode of claim 26 wherein the thin second spacers are a nitride.

28. The gate electrode of claim 27 wherein the thin third spacers are an oxide.

29. The gate electrode of claim 28 wherein the thick fourth spacers are a nitride.

30. The gate electrode of claim 29 wherein the polycide is titanium salicide ($TiSi_2$).

31. A gate electrode formed on a substrate comprising:

an insulative layer formed on a substrate;

a gate layer formed on the insulative layer;

a conductive layer formed on the gate layer;

thin first spacers formed adjacent to opposite sides of the gate layer wherein the thin first spacers are recessed;

thin second spacers formed adjacent to opposite sides of the thin first spacers wherein the thin second spacers are recessed;

thin third spacers formed adjacent to opposite sides of the thin second spacers wherein the thin third spacers are recessed; and,

thick fourth spacers formed adjacent to opposite sides of the thin third spacers wherein the thick fourth spacers are recessed.

32. The gate electrode of claim 31 wherein the insulative layer is an oxide.

33. The gate electrode of claim 32 wherein the gate layer is a polysilicon.

34. The gate electrode of claim 33 wherein the conductive layer is a polycide.

35. The gate electrode of claim 34 wherein the thin first spacers are an oxide.

36. The gate electrode of claim 35 wherein the thin second spacers are a nitride.

37. The gate electrode of claim 36 wherein the thin third spacers are an oxide.

38. The gate electrode of claim 37 wherein the thick fourth spacers are a nitride.

39. The gate electrode of claim 38 wherein the polycide is titanium salicide ($TiSi_2$).

40. A method for forming a gate electrode comprising the steps of:

providing a substrate with an insulative layer deposited thereon;

forming a gate layer on the insulative layer;

depositing a thick first spacer layer on the gate layer and the substrate;

depositing a thick second spacer layer on the thick first spacer layer;

removing a portion of the thick second spacer layer to form thick second spacers adjacent to the thick first spacer layer;

removing a portion of the thick first spacer layer to form recessed thick first spacers adjacent to the gate layer wherein a space is formed between the gate layer and the thick second spacers;

depositing a layer of reactant on the gate layer;

annealing the layer of reactant and the gate layer to form a conductive layer; and,

removing the unreacted reactant layer.

41. The method of claim 40 wherein removing a portion of the thick second spacer layer to form thick second spacers is by anisotropic etching.

42. The method of claim 41 wherein the removing a portion of the thick first spacer layer to form thick first spacers is by isotropic etching.

43. The method of claim 42 wherein the insulative layer is an oxide.

44. The method of claim 43 wherein the gate layer is a polysilicon.

45. The method of claim 44 wherein the reactant is a metal.

46. The method of claim 45 wherein said thick first spacer layer is an oxide.

47. The method of claim 46 wherein said thick second spacer layer is a nitride.

48. The method of claim 47 wherein the conductive layer is a polycide.

49. The method of claim 48 wherein the metal is titanium.

50. The method of claim 49 wherein the polycide is titanium salicide ($TiSi_2$).

51. A method for forming a gate electrode comprising the steps of:
providing a substrate with a gate oxide layer deposited thereon;
forming a gate layer on the insulative layer;
depositing a thin first spacer layer on the gate layer and the substrate;
depositing a thick second spacer layer on the thin first spacer layer;
removing a portion of the thick second spacer layer to form recessed thick second spacers;
removing a portion of the thin first spacer layer to form recessed thin first spacers;
depositing a layer of reactant on the gate layer;
annealing the layer of reactant and the gate layer to form a conductive layer; and,
removing the unreacted reactant layer.

52. The method of claim 51 wherein removing a portion of the thick second spacer layer to form thick second spacers is by anisotropic etching.

53. The method of claim 52 wherein the removing a portion of the thin first spacer layer to form thin first spacers is by isotropic etching.

54. The method of claim 53 wherein the insulative layer is an oxide.

55. The method of claim 54 wherein the gate layer is a polysilicon.

56. The method of claim 55 wherein the reactant is a metal.

57. The method of claim 56 wherein said thin first spacer layer is an oxide.

58. The method of claim 57 wherein said thick second spacer layer is a nitride.

59. The method of claim 58 wherein the conductive layer is a polycide.

60. The method of claim 59 wherein the metal is titanium.

61. The method of claim 60 wherein the polycide is titanium salicide ($TiSi_2$).

62. A method for forming a gate electrode comprising the steps of:

providing a substrate with an insulative layer deposited thereon;

forming a gate layer on the insulative layer;

depositing a thin first spacer layer on the gate layer and the substrate;

depositing a thick second spacer layer on the thin first spacer layer;

removing a portion of the thick second spacer layer to form partially recessed thick second spacers;

removing a portion of the thin first spacer layer to form thin first spacers;

depositing a layer of reactant on the gate layer;

annealing the layer of reactant and the gate layer to form a conductive layer; and,

removing the unreacted reactant layer.

63. The method of claim 62 wherein removing a portion of the thick second spacer layer to form partially recessed thick second spacers further comprises:

removing a first portion of the thick second spacer by anisotropic etching; and,

removing a second portion of the thick second spacer layer by isotropic etching to form thin second spacer walls adjacent to the thin first spacers and in a region adjacent to the conductive layer.

64. The method of claim 63 wherein removing a portion of the thin first spacer layer to form thin first spacers is by anisotropic etching.

65. The method of claim 64 wherein the insulative layer is an oxide.

66. The method of claim 65 wherein the gate layer is a polysilicon.

67. The method of claim 66 wherein the reactant is a metal.

68. The method of claim 67 wherein said thin first spacer layer is an oxide.

69. The method of claim 68 wherein said thick second spacer layer is a nitride.

70. The method of claim 69 wherein the conductive layer is a polycide.

71. The method of claim 70 wherein the metal is titanium.

72. The method of claim 71 wherein the polycide is titanium salicide ($TiSi_2$).

73. A method for forming a gate electrode comprising the steps of :
providing a substrate with an insulative layer deposited thereon;
forming a gate layer on the insulative layer;
depositing a thin first spacer layer on the gate layer and the substrate;
depositing a thin second spacer layer on the thin first spacer layer;
removing a portion of the thin second spacer layer to form thin second spacers;
removing a portion of the thin first spacer layer to form thin first spacers;
depositing a thin third spacer layer;
depositing a thick fourth spacer layer on the thin third spacer layer;
removing a portion of the thick fourth spacer layer to form recessed thick fourth spacers;
removing a portion of the thin third spacer layer to form recessed thin third spacers;
depositing a layer of reactant on the gate layer;

annealing the layer of reactant and the gate layer to form a conductive layer; and,

removing the unreacted reactant layer.

74. The method of claim 73 wherein removing a portion of the thin second spacer layer to form thin second spacers is by anisotropic etching.

75. The method of claim 74 wherein removing a portion of the thin first spacer layer to form thin first spacers is by anisotropic etching.

76. The method of claim 75 wherein removing a portion of the thick fourth spacer layer to form recessed thick fourth spacers further comprises:

removing a first portion of the thick fourth spacer layer by anisotropic etching; and,

removing a second portion of the thick fourth spacer by isotropic etching.

77. The method of claim 76 wherein removing a portion of the thin third spacer layer to form recessed thin third spacers is by anisotropic etching.

78. The method of claim 77 wherein the insulative layer is an oxide.

79. The method of claim 78 wherein the gate layer is a polysilicon.

80. The method of claim 79 wherein the reactant is a metal.

81. The method of claim 80 wherein said thin first spacer layer is an oxide.

82. The method of claim 81 wherein said thin second spacer layer is a nitride.

83. The method of claim 82 wherein said thin third spacer layer is an oxide.

84. The method of claim 83 wherein said thick fourth spacer layer is a nitride.

85. The method of claim 84 wherein the conductive layer is a polycide.

86. The method of claim 85 wherein the metal is titanium.

87. The method of claim 86 wherein the polycide is titanium salicide ($TiSi_2$).

88. A method for forming a gate electrode comprising the steps of :

providing a substrate with an insulative layer deposited thereon;

forming a gate layer on the insulative layer;

depositing a thin first spacer layer on the gate layer and the substrate;

depositing a thin second spacer layer on the thin first spacer layer;

removing a portion of the thin second spacer layer to form thin second spacers;

removing a portion of the thin first spacer layer to form thin first spacers;

depositing a thin third spacer layer;

depositing a thick fourth spacer layer on the thin third spacer layer;

removing a portion of the thick fourth spacer layer to form recessed thick fourth spacers;

removing a portion of the thin third spacer layer to form recessed third spacers;

forming a protective layer on the substrate and gate layer;

removing a portion of the thin second spacers to form recessed thin second spacers;

removing the protective layer and removing a portion of the thin first spacers to form recessed thin first spacers;

depositing a layer of reactant on the gate layer;

annealing the layer of reactant and the gate layer to form a conductive layer; and,

removing the unreacted reactant layer.

89. The method of claim 88 wherein removing a portion of the thin second spacer layer to form thin second spacers is by anisotropic etching.

90. The method of claim 89 wherein removing a portion of the thin first spacer layer to form thin first spacers is by anisotropic etching.

91. The method of claim 90 wherein removing a portion of the thick fourth spacer layer to form recessed thick fourth spacers further comprises:

removing a first portion of the thick fourth spacer layer by anisotropic etching; and,

removing a second portion of the thick fourth spacer layer by isotropic etching.

92. The method of claim 91 wherein removing a portion of the thin third spacer layer to form recessed thin third spacers is by anisotropic etching.

93. The method of claim 92 wherein removing a portion of the thin second spacers to form recessed thin second spacers is by isotropic etching.

94. The method of claim 93 wherein removing the protective layer and removing a portion of the thin first spacers to form recessed thin first spacers is by isotropic etching.

95. The method of claim 94 wherein the insulative layer is an oxide.

96. The method of claim 95 wherein the gate layer is a polysilicon.

97. The method of claim 96 wherein the reactant is a metal.

98. The method of claim 97 wherein the thin first spacer layer is an oxide.

99. The method of claim 98 wherein the thin second spacer layer is a nitride.

100. The method of claim 99 wherein the thin third spacer layer is an oxide.

101. The method of claim 100 wherein the thick fourth spacer layer is a nitride.

102. The method of claim 101 wherein the protective layer is an oxide.

103. The method of claim 101 wherein the conductive layer is a polycide.

104. The method of claim 102 wherein the metal is titanium.

105. The method of claim 103 wherein the polycide is titanium salicide ($TiSi_2$).

106. A method for forming a gate electrode comprising the steps of :

providing a substrate with an insulative layer deposited thereon;

forming a gate layer on the insulative layer;

depositing a thin first spacer layer on the gate layer and the substrate;

depositing a thin second spacer layer on the thin first spacer layer;

removing a portion of the thin second spacer layer to form thin second spacers;

removing a portion of the thin first spacer layer to form thin first spacers;

depositing a thin third spacer layer;

depositing a thick fourth spacer layer on the thin third spacer layer;

removing a portion of the thick fourth spacer layer to form recessed thick fourth spacers;

removing a portion of the thin third spacer layer to form recessed third spacers;

removing a portion of the thin second spacers to form recessed thin second spacers;

removing a portion of the thin first spacers to form recessed thin first spacers;

depositing a layer of reactant on the gate layer;

annealing the layer of reactant and the gate layer to form a conductive layer; and,

removing the unreacted reactant layer.

107. The method of claim 105 wherein removing a portion of the thin second spacer layer to form thin second spacers is by anisotropic etching.

108. The method of claim 106 wherein removing a portion of the thin first spacer layer to form thin first spacers is by anisotropic etching.

109. The method of claim 107 wherein removing a portion of the thick fourth spacer layer to form recessed thick fourth spacers further comprises:

removing a first portion of the thick fourth spacer layer by anisotropic etching; and,

15 removing a second portion of the thick fourth spacer layer by isotropic etching.

110. The method of claim 108 wherein removing a portion of the thin third spacer layer to form recessed thin third spacers is by anisotropic etching.

111. The method of claim 109 wherein removing a portion of the thin second spacers to form recessed thin second spacers is by isotropic etching.

112. The method of claim 110 wherein removing a portion of the thin first spacers to form recessed thin first spacers is by isotropic etching.

113. The method of claim 111 wherein the insulative layer is an oxide.

114. The method of claim 112 wherein the gate layer is a polysilicon.

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115. The method of claim 113 wherein the reactant is a metal.

116. The method of claim 114 wherein the thin first spacer layer is an oxide.

117. The method of claim 115 wherein the thin second spacer layer is a nitride.

118. The method of claim 116 wherein the thin third spacer layer is an oxide.

119. The method of claim 117 wherein the thick fourth spacer layer is a nitride.

120. The method of claim 118 wherein the conductive layer is a polycide.

121. The method of claim 119 wherein the metal is titanium.

122. The method of claim 120 wherein the polycide is titanium salicide ($TiSi_2$).

ABSTRACT OF THE DISCLOSURE

A method and device for improved salicide resistance in polysilicon gates under .20 μm. The several embodiments of the invention provide for formation of gate electrode structures with recessed and partially recessed spacers. One embodiment, provides a gate electrode structure with recessed thick inner spacers and thick outer spacers. Another embodiment provides a gate electrode structure with recessed thin inner spacers and recessed thick outer spacers. Another embodiment provides a gate electrode structure with thin inner spacers and partially recessed outer spacers. Another embodiment provides a gate electrode structure with two spacer stacks. The outermost spacer stack with recessed thin inner spacers and recessed thick outer spacers. The inner spacer stack with thin inner spacers and thin outer spacers. Another embodiment provides a gate electrode structure with two spacer stacks. The outermost spacer stack with recessed thin inner spacers and recessed thick outer spacers. The inner spacer stack with recessed thin inner spacers and recessed thin outer spacers.

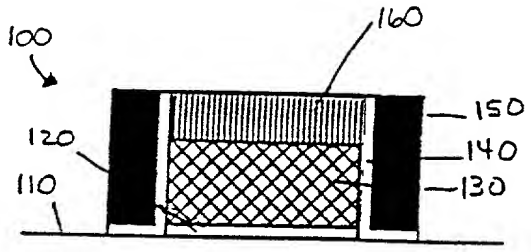

FIG. 1A
(PRIOR ART)

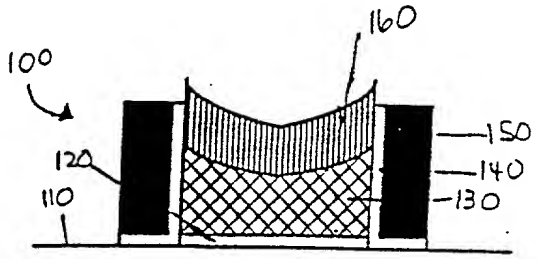

FIG. 1B
(PRIOR ART)

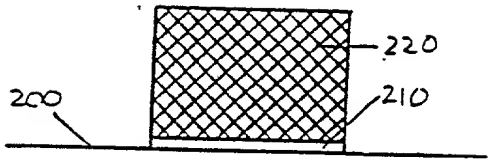

FIG. 2A

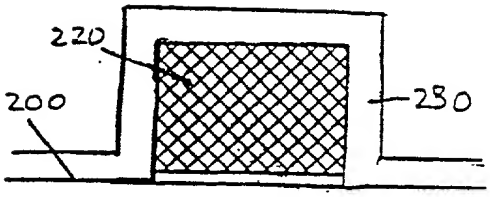

FIG. 2B

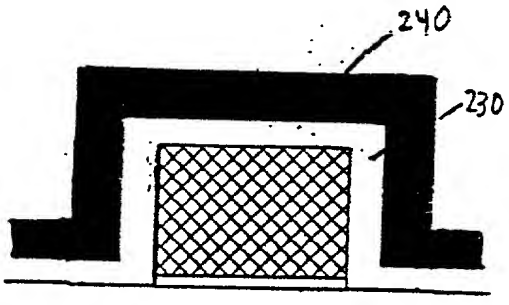

FIG. 2C

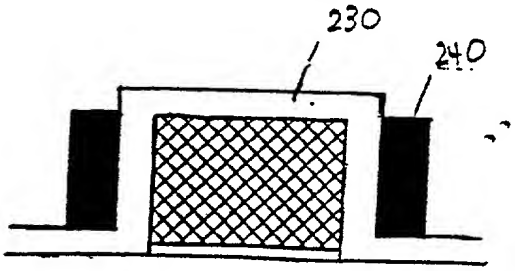

FIG. 2D

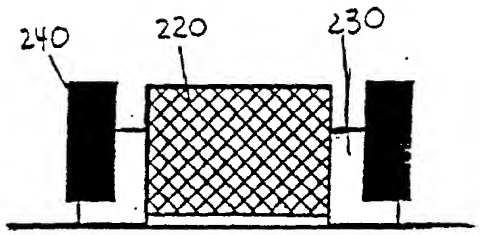

FIG. 2E

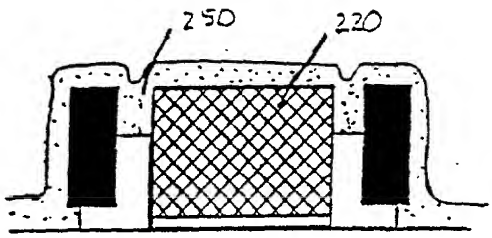

FIG 2F

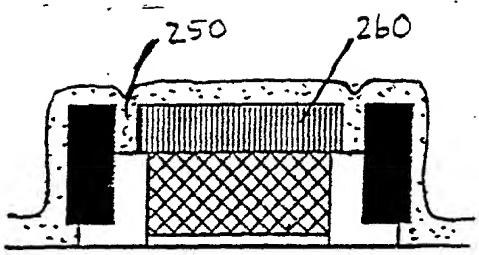

FIG. 2G

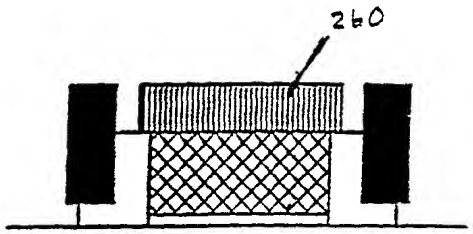

FIG. 2H

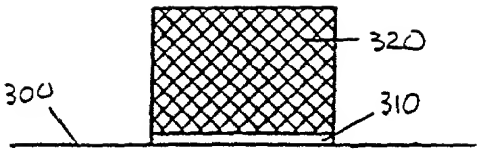

FIG. 3A

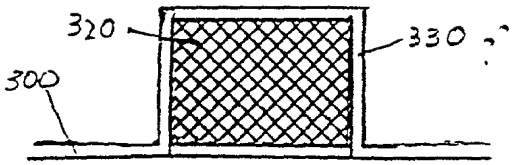

FIG. 3B

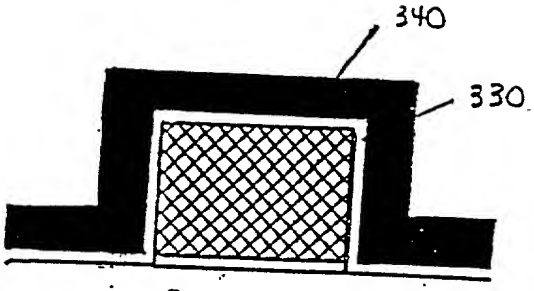

FIG. 3C

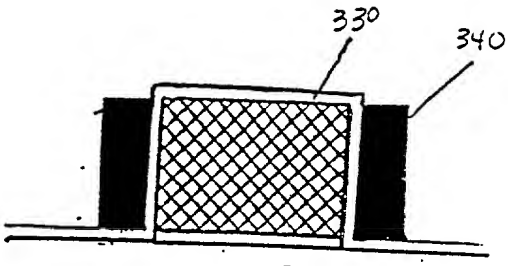

FIG. 3D

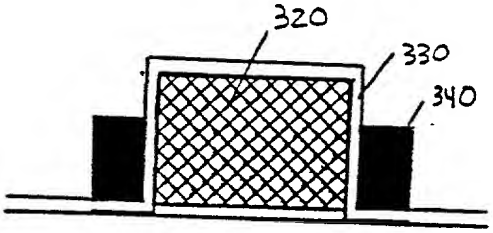

FIG. 3E

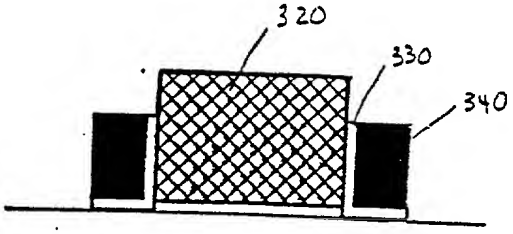

FIG. 3F

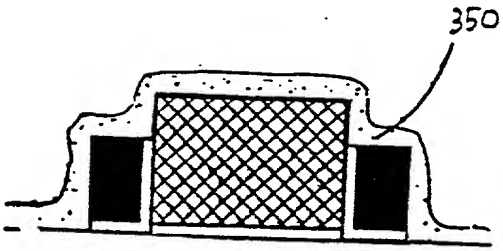

FIG. 3G

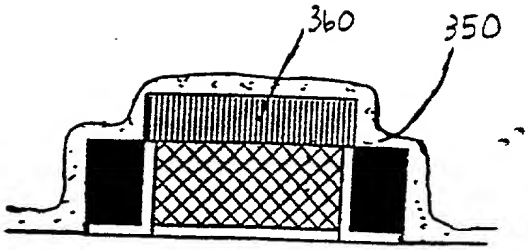

FIG. 3H

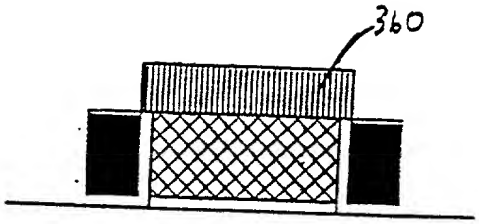

FIG. 3I

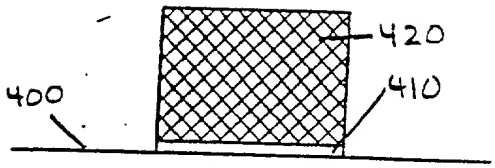

FIG. 4A

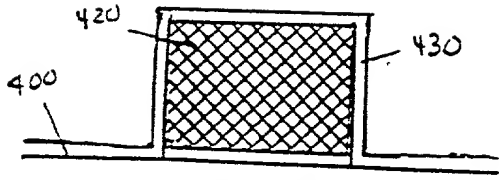

FIG. 4B

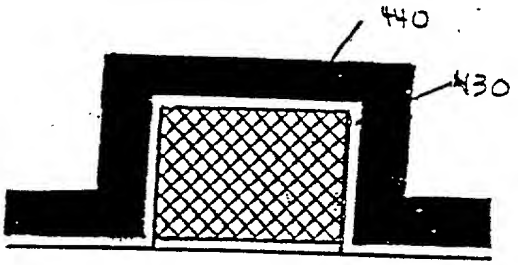

FIG. 4C

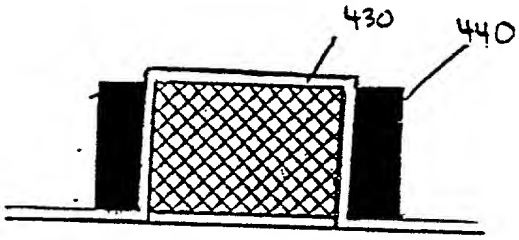

FIG. 4D

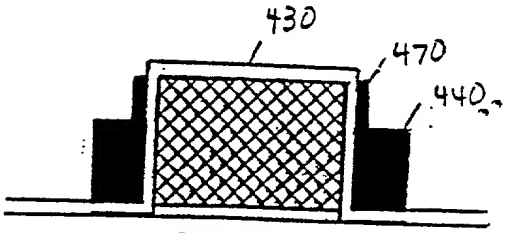

FIG. 4E

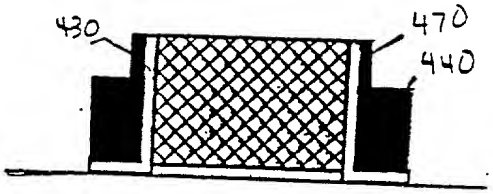

FIG. 4F

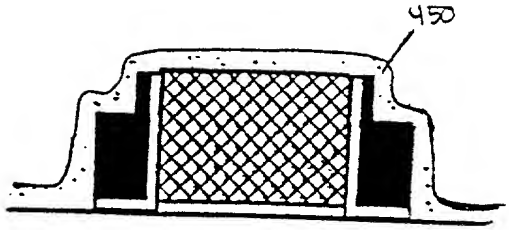

FIG. 4G

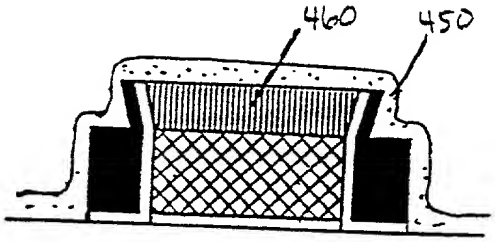

FIG. 4H

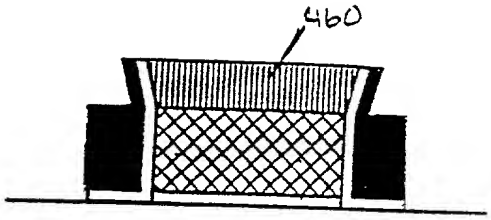

FIG. 4I

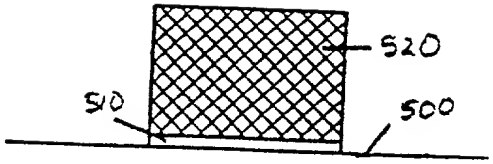

FIG. 5A

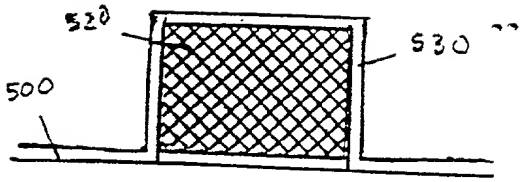

FIG. 5B

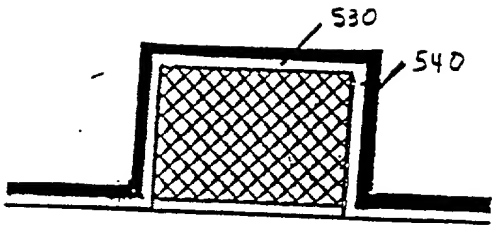

FIG. 5C

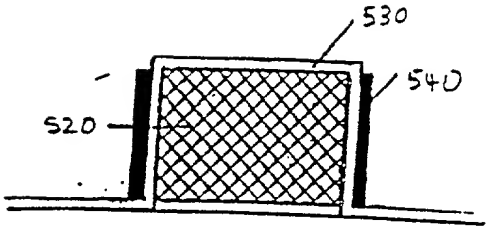

FIG. 5D

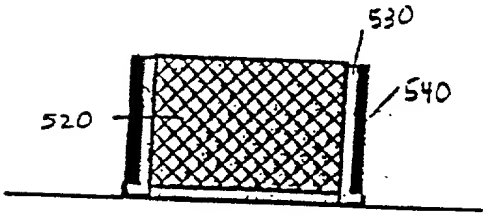

FIG. 5E

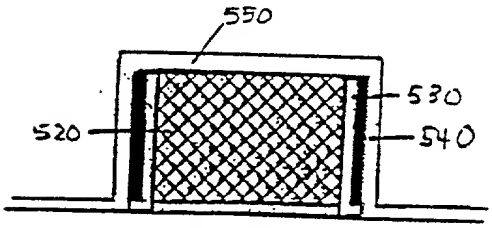

FIG. 5F

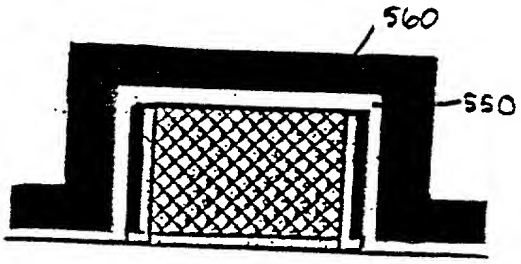

FIG. 5G

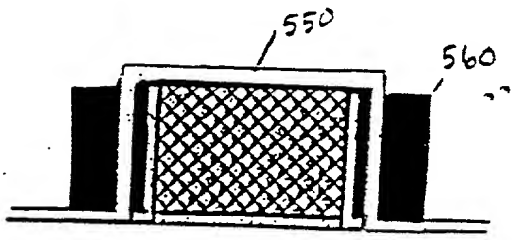

FIG. 5H

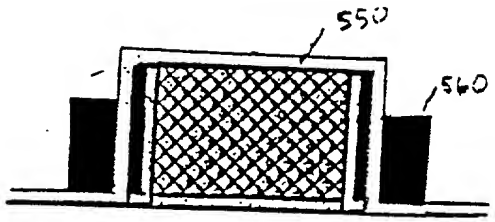

FIG. 5I

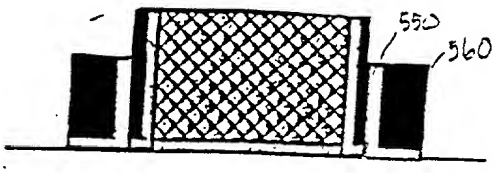

FIG. 5J

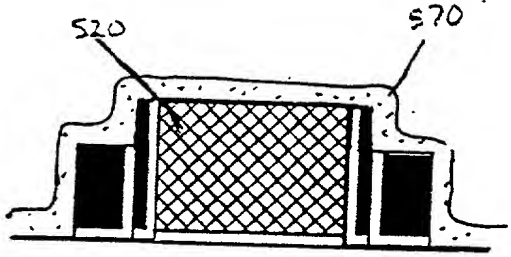

FIG. 5K

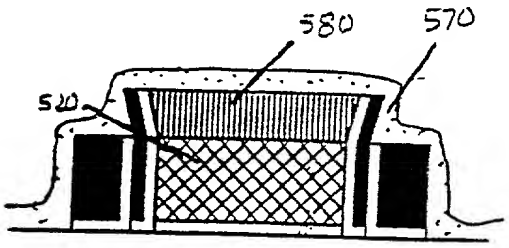

FIG. 5L

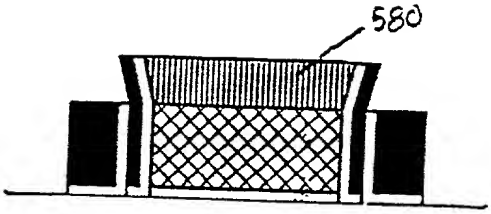

FIG. 5M

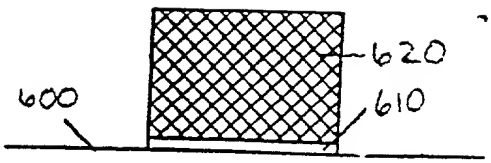

FIG. 6A

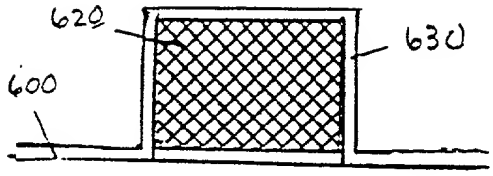

FIG. 6B

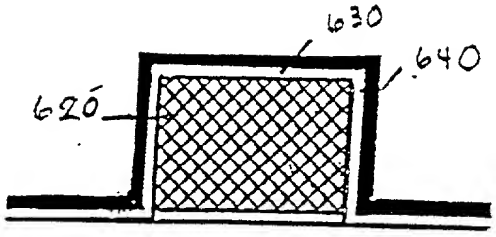

FIG. 6C

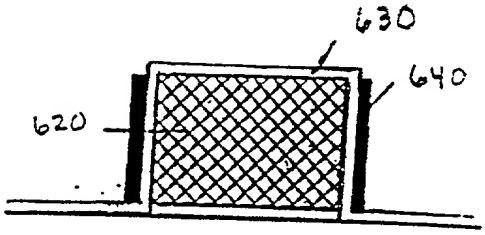

FIG. 6D

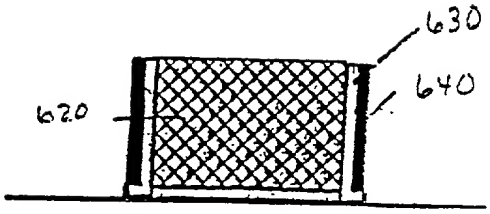

FIG. 6E

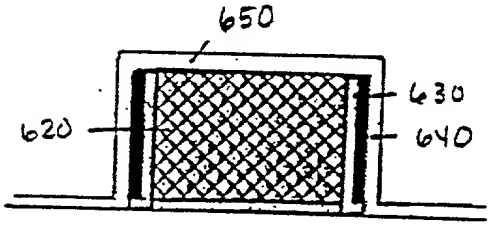

FIG. 6F

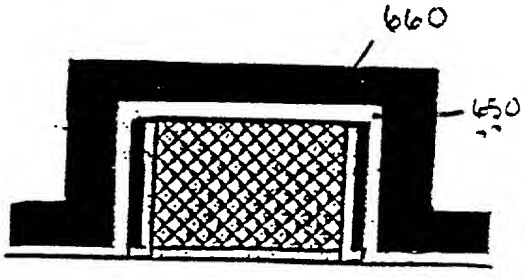

FIG. 6G

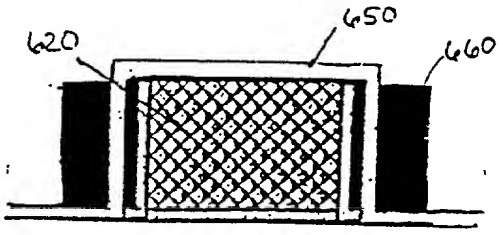

FIG. 6H

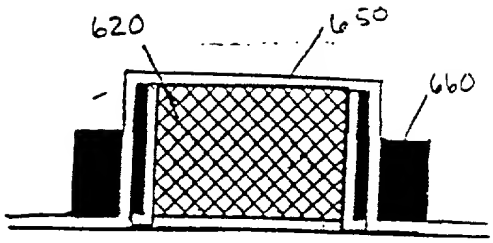

FIG. 6I

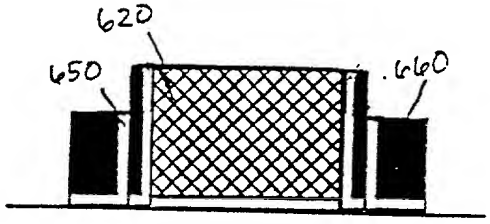

FIG. 6J

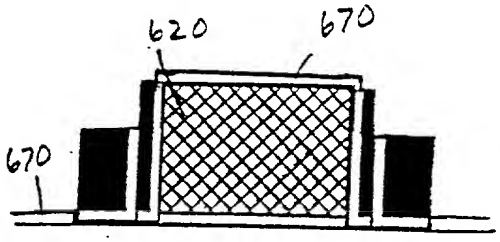

FIG. 6K

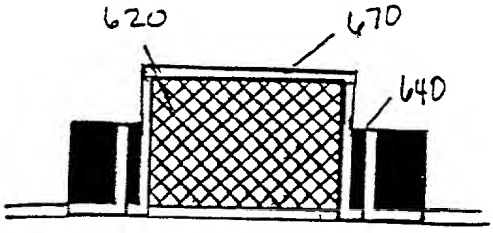

FIG. 6L

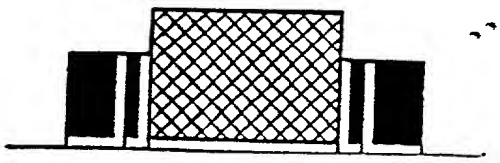

FIG. 6M

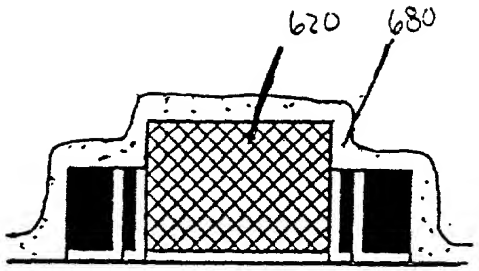

FIG. 6N

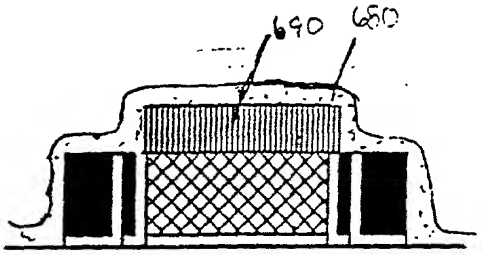

FIG. 6O

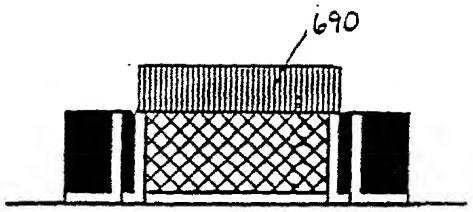

FIG. 6P

Attorney's Docket No.: 042390.P5488 PATENT

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION
(FOR **INTEL CORPORATION** PATENT APPLICATIONS)

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below, next to my name.

I believe I am the original, first, and sole inventor (if only one name is listed below) or an original, first, and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

A METHOD AND DEVICE FOR IMPROVED SALICIDE RESISTANCE ON POLYSILICON GATES

the specification of which

_____ is attached hereto.
__X__ was filed on November 13, 1998 as
United States Application Number 09/191,729
or PCT International Application Number _____
and was amended on _____.
(if applicable)

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claim(s), as amended by any amendment referred to above. I do not know and do not believe that the claimed invention was ever known or used in the United States of America before my invention thereof, or patented or described in any printed publication in any country before my invention thereof or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, and that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve months (for a utility patent application) or six months (for a design patent application) prior to this application.

I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, Section 119(a)-(d), of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)			Priority Claimed	
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No

I hereby claim the benefit under title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below

(Application Number)	Filing Date
(Application Number)	Filing Date

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application:

(Application Number)	Filing Date	(Status -- patented, pending, abandoned)
(Application Number)	Filing Date	(Status -- patented, pending, abandoned)

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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Title 37, Code of Federal Regulations, Section 1.56
Duty to Disclose Information Material to Patentability

(a) A patent by its very nature is affected with a public interest. The public interest is best served, and the most effective patent examination occurs when, at the time an application is being examined, the Office is aware of and evaluates the teachings of all information material to patentability. Each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the Office, which includes a duty to disclose to the Office all information known to that individual to be material to patentability as defined in this section. The duty to disclosure information exists with respect to each pending claim until the claim is cancelled or withdrawn from consideration, or the application becomes abandoned. Information material to the patentability of a claim that is cancelled or withdrawn from consideration need not be submitted if the information is not material to the patentability of any claim remaining under consideration in the application. There is no duty to submit information which is not material to the patentability of any existing claim. The duty to disclosure all information known to be material to patentability is deemed to be satisfied if all information known to be material to patentability of any claim issued in a patent was cited by the Office or submitted to the Office in the manner prescribed by §§1.97(b)-(d) and 1.98. However, no patent will be granted on an application in connection with which fraud on the Office was practiced or attempted or the duty of disclosure was violated through bad faith or intentional misconduct. The Office encourages applicants to carefully examine:

(1) Prior art cited in search reports of a foreign patent office in a counterpart application, and

(2) The closest information over which individuals associated with the filing or prosecution of a patent application believe any pending claim patentably defines, to make sure that any material information contained therein is disclosed to the Office.

(b) Under this section, information is material to patentability when it is not cumulative to information already of record or being made or record in the application, and

(1) It establishes, by itself or in combination with other information, a prima facie case of unpatentability of a claim; or

(2) It refutes, or is inconsistent with, a position the applicant takes in:

(i) Opposing an argument of unpatentability relied on by the Office, or

(ii) Asserting an argument of patentability.

A prima facie case of unpatentability is established when the information compels a conclusion that a claim is unpatentable under the preponderance of evidence, burden-of-proof standard, giving each term in the claim its broadest reasonable construction consistent with the specification, and before any consideration is given to evidence which may be submitted in an attempt to establish a contrary conclusion of patentability.

(c) Individuals associated with the filing or prosecution of a patent application within the meaning of this section are:

(1) Each inventor named in the application;

(2) Each attorney or agent who prepares or prosecutes the application; and

(3) Every other person who is substantively involved in the preparation or prosecution of the application and who is associated with the inventor, with the assignee or with anyone to whom there is an obligation to assign the application.

(d) Individuals other than the attorney, agent or inventor may comply with this section by disclosing information to the attorney, agent, or inventor.